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Substitute for f	om 1449A/B/PTO			Application Number	Unassigned	
INIE	ORMATION	DISC	N OSLIDE	Filing Date	January 28, 2004	
	•			First Named Inventor	Yutaka ARIMA	
STA	TEMENT B	Y AP	PLICANT	Group Art Unit	Unassigned	
	(Use as many shee	ets as nec	cessary)	Examiner Name	Unassigned	
Sheet	1	of	1	Attorney Docket Number	402952/SAKAI	

U.S. PATENT DOCUMENTS						
		U.S. Palent Document		U.S. Palent Document		
Examiner Initials	Doc. No.	Application or Patent Number	Kind Code	Name of Patentee or Applicant	Date of Publication	Filing Date If Appropriate
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FOREIGN PATENT DOCUMENTS							
Foreign Patent Document						Translation	
Doc. No.	Office	Application or Patent Number	Kind Code	Name of Patentee or Applicant	Date of Publication	Yes	No*+
A 2	JP	2002-222944 A		K.K. KITAKYUSYU TECHNOLOGY CENTER	8/9/2002		X+
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	OTHER • NON PATENT LITERATURE DOCUMENTS			
Examiner Initials Doc. No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item			
	(book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number (s), publisher, city and/or country where published.	Yes	No*+	
А3	T. SHIBATA et al., "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations" <i>IEEE Transactions on Electron Devices, June 1992, pp. 1444-1455, Vol. 39(6)</i>			
A 4	T. HASHIMOTO et al., "Thin Film Effects of Double-Gate Polysilicon MOSFET," Extended Abstracts of the 22 nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 393-396, JAPAN			
A 5	T. HIRAMOTO et al., "Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias," <i>IEICE Trans. Electron, February 2000, pp. 161-169, Vol. E84-C(2).</i>			
	A3	Doc. No. Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number (s), publisher, city and/or country where published. A.3 T. SHIBATA et al., "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations" IEEE Transactions on Electron Devices, June 1992, pp. 1444-1455, Vol. 39(6) T. HASHIMOTO et al., "Thin Film Effects of Double-Gate Polysilicon MOSFET," Extended Abstracts of the 22 nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 393-396, JAPAN T. HIRAMOTO et al., "Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias," IEICE Trans. Electron, February 2000,	Doc. No. Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number (s), publisher, city and/or country where published. T. SHIBATA et al., "A Functional MOS Transistor Featuring Gate-Level Weighted Sum and Threshold Operations" IEEE Transactions on Electron Devices, June 1992, pp. 1444-1455, Vol. 39(6) T. HASHIMOTO et al., "Thin Film Effects of Double-Gate Polysilicon MOSFET," Extended Abstracts of the 22 nd (1990 International) Conference on Solid State Devices and Materials, Sendai, 1990, pp. 393-396, JAPAN T. HIRAMOTO et al., "Low Power and Low Voltage MOSFETs with Variable Threshold Voltage Controlled by Back-Bias," IEICE Trans. Electron, February 2000,	

Examiner Signature	Solution	Date Considered 9-9-2004

A concise statement of relevance is being submitted in fleu of a translation. 37 CFR 1.98(a)(3).
 An English-language equivalent/patent, or an English-language abstract, or an English-language version of the search report or action by a foreign patent office in a counterpart foreign application indicating the degree of relevance found by the foreign office is being submitted in fleu of a concise explanation of relevance under 37 CFR 1.98(a)(3).